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A HIGH CMRR, LOW-POWER OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH 0.18µM CMOS TECHNOLOGY

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ABSTRACT

This paper represent an Operational Transconductance Amplifier (OTA) which is a basic building block in many analog circuit such as in data converter's (ADC &DAC), biquad filter design and instrumentation amplifiers. This OTA is implemented using 0.18µm CMOS technology with cadence environment and it has ±1.25v power supply with biasing current of 33nA. OTA has been simulated with virtuoso simulator and simulation results are measured. Post layout simulations for a 1 pF load capacitance shows that OTA achieves a gain bandwidth of 270 KHz at a phase margin 68.43° with 90.27 dB DC gain. This OTA is having CMRR of 154 dB, PSRR of 119 dB, Power dissipation of 29.58nW and Slew Rate 2.49 V/µsec.

KEYWORDS: Cadence, Operational Transconductance Amplifier (OTA), CMRR, PSRR, DC Gain, Unity Gain Bandwidth (UGBW), CMFB

INTRODUCTION

The operational amplifiers (OPAMP) are basic building blocks in implementing a variety of analog Circuits such as amplifiers, filters, integrators, differentiators, summers, oscillators etc. For higher frequencies, however, OPAMP designs become difficult due to their frequency limit [2], [3]. At those high frequencies, operational transconductance amplifiers (OTAs) are deemed to be promising to replace OPAMPS as the building blocks [1]-[11].

Fully differential OTAs are preferred because they provide larger signal swing, better distortion performance, better CM noise and supply noise rejection. The Fully differential OTAs require a common-mode feedback (CMFB) circuit.

In Reference [4] a CMFB circuit which operated at 0.5 V by using two resistors to sense the output CM levels was designed. But this structure increases the die area and reduces the gain due to longer loads the OTA. To overcome some of these problems, a CMFB circuit has been reported [5].

This structure uses of four PMOS and two NMOS transistors. The NMOS devices is a bulk-input current mirror, which compares the current of the PMOS devices and then difference of these current is fed to the gate of the input transistors for controlling of the output CM voltages. This paper is given a novel continuous-time CMFB circuit that is able to operate with an ultra low-voltage supply.

So there are several different OTA's are used in which this OTA (shown in figure 1) is a simple OTA with low supply voltage of VDD= +1.25V and VSS= -1.25Vand high gain. The design parameters of this OTA are shown in below table 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

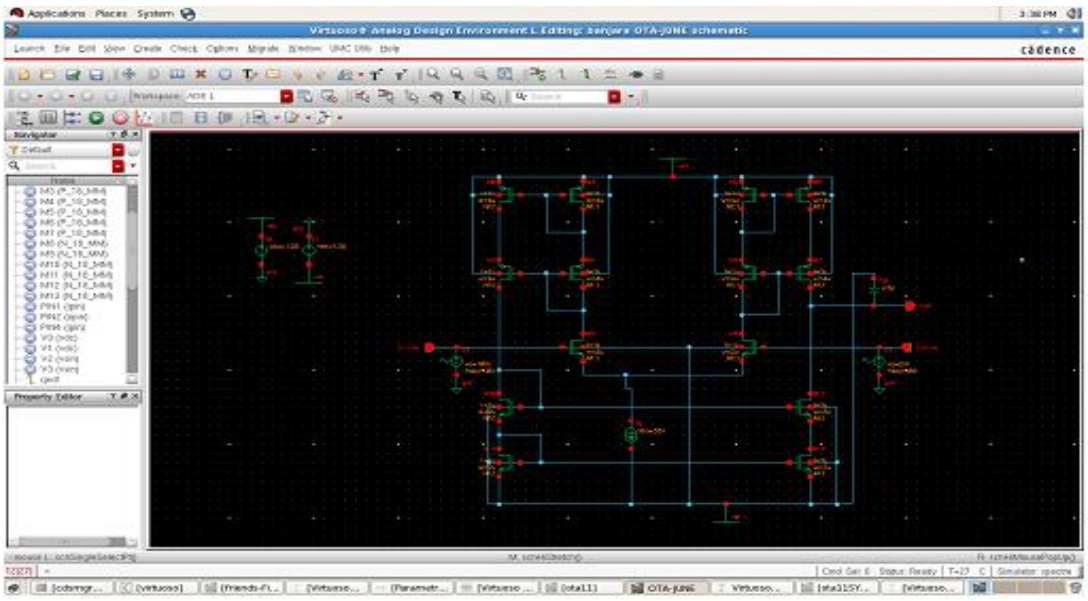

Figure 1: Schematic of OTA

Table 1: Dimensions of CMOS Transistors

Transistor Type	Transistor Name	W(µm)	L(µm)
PMOS	M0, M1, M2, M3, M4, M5, M6, M7	4	1
NMOS	M8, M9, M10, M11, M12, M13	2	1

SIMULATION RESULTS OF PROPOSED OTA

The design of this OTA is done using Cadence Tool. The simulations were performed under normal condition (room temperature) on Cadence Spectre Environment using UMC 0.18 µm CMOS technology with ±1.25v power supply. The AC simulation results are shown in Figure 2. It shows that the dc gain is 90.27 dB and the bandwidth is 270 KHz. The phase margin is about 68.43°. Furthermore, Table II summarizes the simulated performance of this OTA.

Figure 3 shows schematic for CMRR analysis of OTA. The change in CMRR with frequency is shown in figure 4 which is 154 dB. Figure 5 shows schematic for PSRR analysis. The variation in PSRR is shown in figure 6 which is 119 dB.

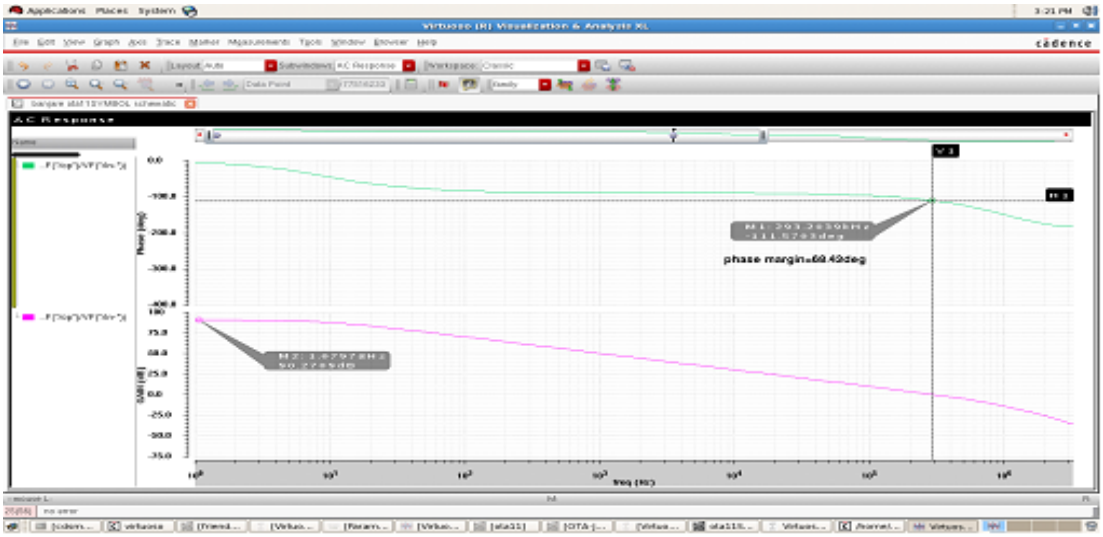

Figure 2: AC Response of OTA

Table 2: Specifications of Proposed OTA Compared with Similar Works

Specification	[4]	[5]	This Design
Technology	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
Supply voltage	0.5v	0.5v	±1.25v
Open-loop DC Gain	62 dB	65 dB	90.27 dB
Phase margin	60°	65°	68.43°
Gain margin	NA	NA	30 dB
Load Capacitors	20 pf	20 pf	1 pf
Power Consumption	110 µW	28 µW	29.58nW
Unity Gain BW	10 MHz	550 KHz	270 KHz
CMRR	NA	NA	154 dB
PSRR	NA	NA	119 dB
Slew Rate	NA	NA	2.49v/µsec

NA. Not Available

COMMON MODE REJECTION RATIO (CMRR)

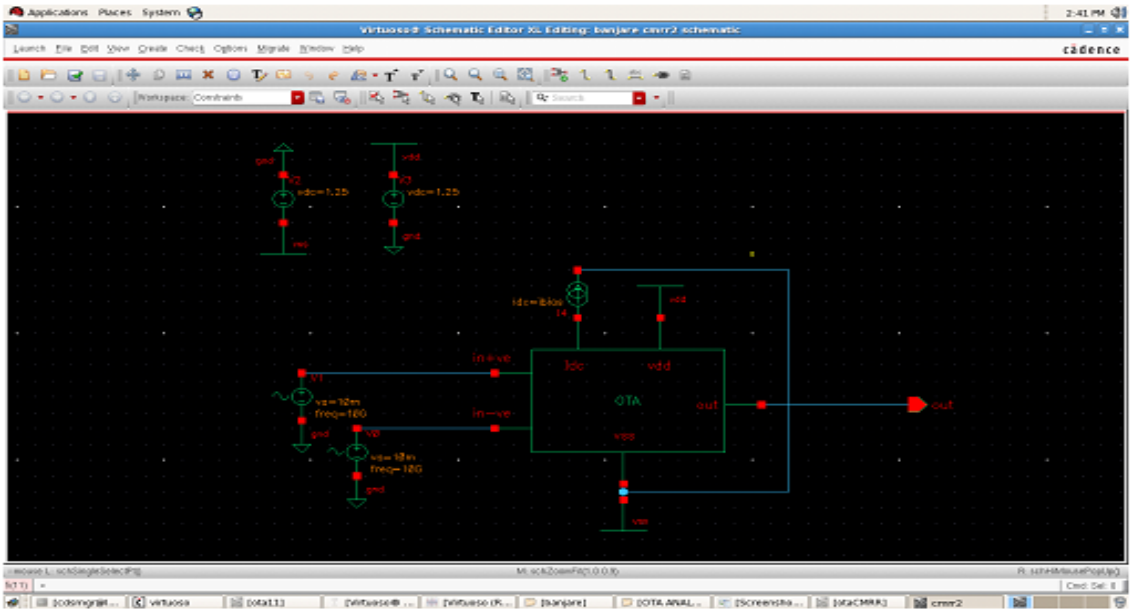

Figure 3: Schematic for CMRR

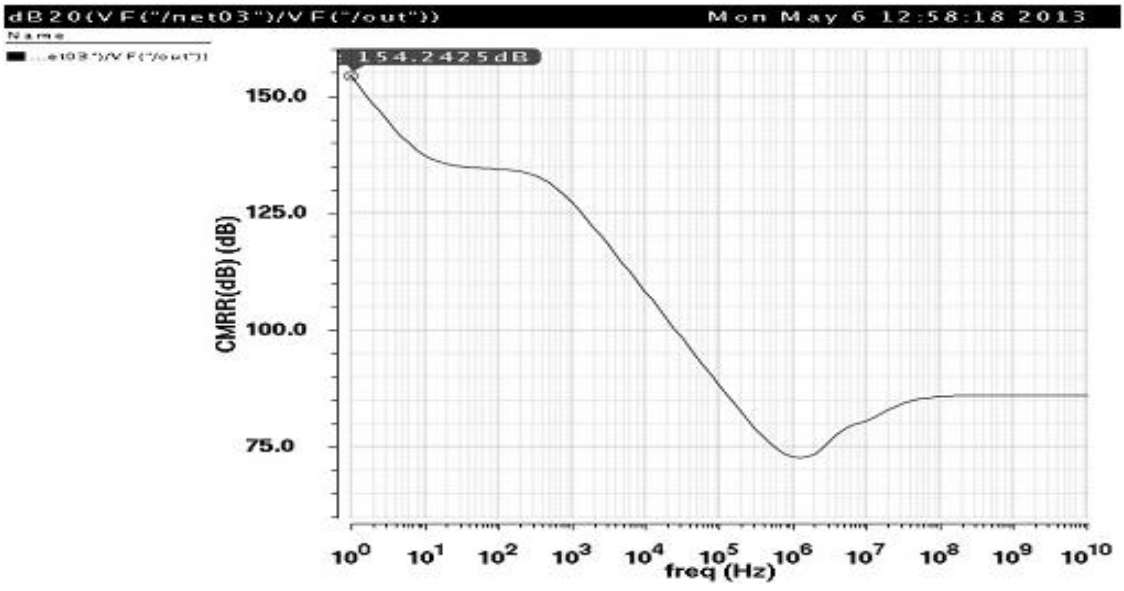

Figure 4: CMRR versus Frequency

POWER SUPPLY REJECTION RATIO (PSRR)

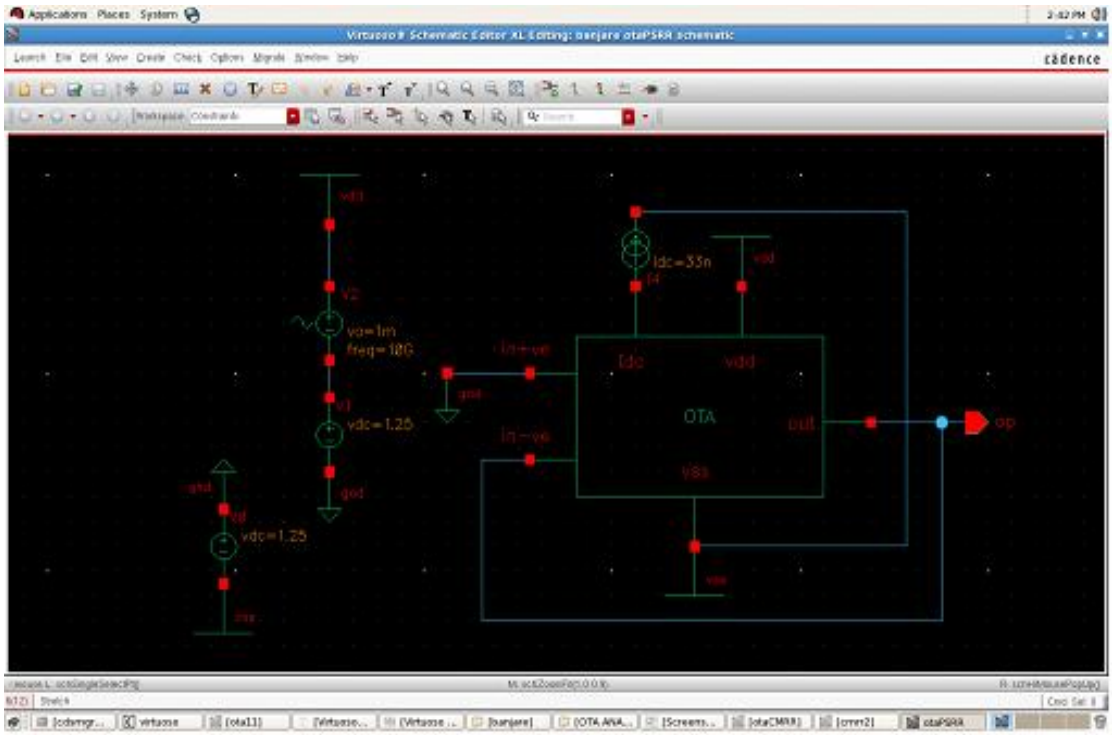

Figure 5: Schematic for PSRR

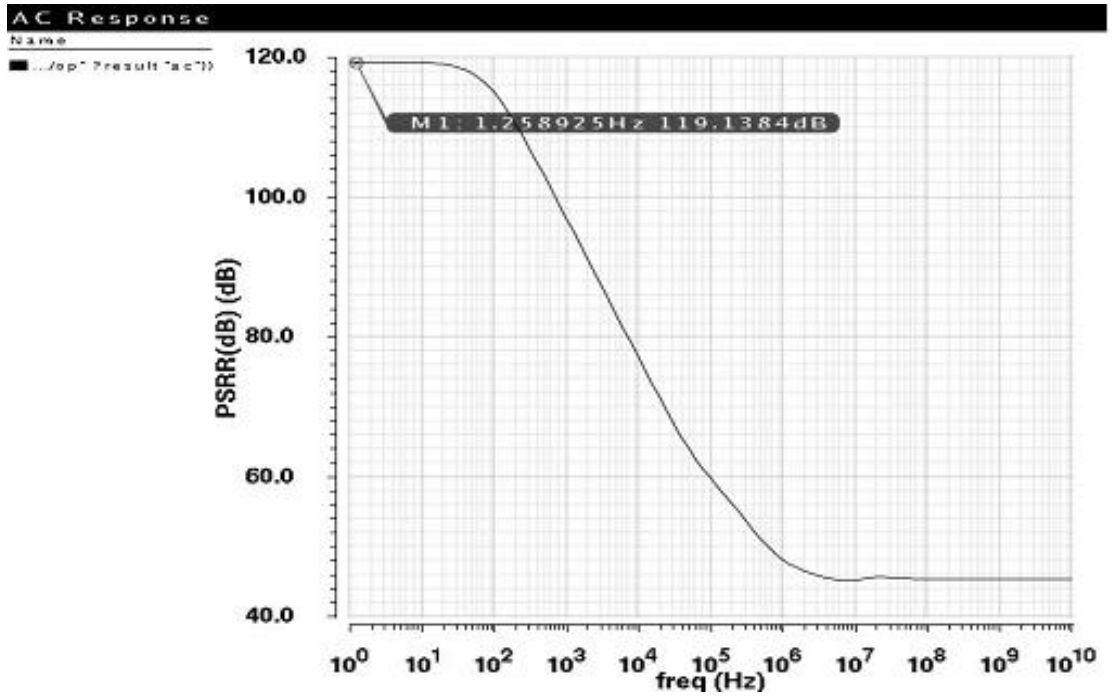

Figure 6: PSRR versus Frequency

CONCLUSIONS

In this paper a simple OTA configuration for low-voltage and low-power application in 0.18 µm CMOS process has been presented. A complete analysis of this OTA is presented in this paper which shows how this circuit leads to a high gain and high CMRR. With the load capacitor of 1 pF, the design demonstrates a dc Gain of 90.27 dB with a bandwidth of 270 KHz and high CMRR of 154 dB. So this work can be used in process controller, physical transducers and small battery operated devices, continuous-time filter design, and ADC design and instrumentation amplifiers.

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